AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.(Currently Amended) A system for generating and acquiring pseudo-noise (PN) spread signals, the system comprising:

a transmitter, wherein the transmitter comprises:

a first clock generator,

at least three first pseudo-noise (PN) component code generators coupled to the first clock generator;

a logic combiner coupled to the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock generator;

a second clock generator, wherein the second clock is adapted to synchronize with the first clock generator;

a second M-bit counter coupled to the second clock generator;

a receiver, the receiver adapted to receive signals from the transmitter, comprising:

a link control processor;

a modulator/demodulator controller coupled to the link control processor;

a first receiver clock generator;

at least three first receiver pseudo-noise (PN) component code generators coupled to the first receiver clock generator;

a despreader coupled to one of the at least three first receiver PN component code generators;

a receiver logic combiner coupled to the at least three first receiver PN component code generators, the receiver logic combiner adapted to generate ~~the~~ a composite PN code;

a first receiver N-bit counter coupled to the first receiver clock generator;

a second receiver clock generator, wherein the second receiver clock generator is adapted to synchronize with the first receiver clock; and

a second receiver M-bit counter coupled to the second receiver clock generator.

2.(Original) A system as in claim 1 wherein the first clock generator comprises a first direct digital synthesizer.

3.(Currently Amended) A system as in claim 1 wherein the logic combiner comprises a MAND logic combiner that logically XOR combines an output of one of the PN code generators with a logical AND result of at least two other of the PN code generators.

4.(Currently Amended) A system as in claim 1 wherein the logic combiner comprises a MAJ logic combiner that logically XOR combines all logical AND combinations of unique pairs of PN code generator outputs.

5.(Original) A system as in claim 1 wherein the at least three first PN component code generators comprise four first PN component code generators.

6.(Original) A system as in claim 1 wherein the at least three first receiver PN component code generators comprise four first receiver PN component code generators.

7.(Original) A system as in claim 1 wherein the second clock generator comprises a crystal reference oscillator.

8.(Canceled)

9.(Original) A system as in claim 1 wherein the second receiver clock generator comprises a second crystal reference oscillator.

10.(Canceled)

11.(Original) A system as in claim 1 wherein the second N-bit counter coupled to the second clock comprises at least a 40-bit counter.

12.(Original). A system as in claim 1 wherein the second receiver N-bit counter comprises at least a 40-bit counter.

13.(Currently Amended) A method for generating and acquiring pseudo-noise (PN) composite spread signals, the method comprising the steps of:

at a transmitter:

providing a PN clock source, the PN clock source having a predetermined cycle rate;

using the PN clock source to generate at least three transmit PN component codes, wherein the step of generating the at least three transmit PN component codes further comprises the steps of:

initializing a first counter, wherein the first counter is adapted to count the PN clock source cycles;

logically combining the at least three transmit PN component codes to produce a transmit PN composite code;

providing an oscillatory reference source, the oscillatory reference source having predetermined cycles;

initializing a second counter, wherein the second counter is adapted to count the cycles of the oscillatory reference source;

determining a transmitter delta phase in accordance with counts from the first counter and the second counter;

transmit PN composite coding the transmitter delta phase and a cycle count of the second counter ~~count~~;

transmitting the transmit PN composite coded transmitter delta phase and the PN composite coded cycle count of the second counter ~~count~~ at a predetermined rate;

at a receiver:

receiving the transmitted signal;

partially correlating the ~~transmitted~~ received signal; and

determining a receive PN composite code slip for chip aligning a receive ~~receiver~~ PN composite code with the transmit ~~transmitter~~ PN composite code.

14.(Currently Amended) A method as in claim 13 wherein the step of providing the PN clock source ~~further~~ comprises the step of providing a direct digital synthesizer.

15.(Currently Amended) A method as in claim 13 wherein the step of generating the at least three transmit PN component codes ~~further~~ comprises the step of generating one of the at least three transmit PN component codes with predetermined auto-correlation properties.

16.(Currently Amended) A method as in claim 13 wherein the step of generating at least three transmit PN component codes ~~further~~ comprises the step of generating four transmit PN component codes.

17.(Currently Amended) A method as in claim 16 wherein the step of combining the four transmit PN component codes ~~further~~ comprises ~~the step of~~ ~~MAND~~ logically combining the four transmit PN component codes X, Y, Z_1 and Z_2 according to:

$$(X \oplus (Y \bullet (Z_1 \oplus Z_2)).$$

18.(Currently Amended) A method as in claim 16 wherein the step of combining the four transmit PN component codes ~~further~~ comprises ~~the step of MAJ~~ logically combining the four transmit PN component codes X, Y, Z_1 and Z_2 according to:

$$(X \bullet Y) \oplus (X \bullet Z_1) \oplus (X \bullet Z_2) \oplus (Y \bullet Z_1) \oplus (Y \bullet Z_2) \oplus (Z_1 \bullet Z_2).$$

19.(Currently Amended) A method as in claim 13 wherein the step of providing the oscillatory reference source ~~further~~ comprises ~~the step of~~ providing a crystal ~~oscillator~~ oscillatory reference source.

20.(Currently Amended) A method as in claim 19 wherein the step of providing the crystal oscillator reference source ~~further~~ comprises ~~the step of~~ providing a 10MHz reference source.

21.(Currently Amended) A method as in claim 13 wherein the step of providing the oscillatory reference source ~~further~~ comprises ~~the step of~~ providing an atomic reference source.

22.(Currently Amended) A method as in claim 13 wherein the step of initializing the second counter ~~further~~ comprises ~~the step of~~ initializing the second counter at substantially the same time as initializing the first counter.

23.(Currently Amended) A method as in claim 13 wherein the step of partially correlating the ~~transmitted~~ received signal ~~further~~ comprises ~~the steps of~~:

providing one of ~~the~~ at least three receive PN component codes; and

correlating the one of the at least three receive PN component codes with the ~~transmitted~~ received signal.

24.(Currently Amended) A method as in claim 23 wherein the step of determining the receive PN composite code slip for chip aligning further comprises ~~the steps of~~:

providing a PN receiver clock source, the PN receiver clock source having a predetermined cycle rate;

using the PN receiver clock source to generate ~~the~~ at least three receive PN component codes, wherein the step of generating the at least three receive PN component codes ~~further~~ comprises the steps of:

initializing a receiver first counter, wherein the receiver first counter is adapted to count the PN receiver clock source cycles;

logically combining the at least three receive PN component codes to produce the receive PN composite code;

providing a receiver oscillatory reference source, the receiver oscillatory reference source having predetermined cycles;

initializing a receiver second counter, wherein the receiver second counter is adapted to count the cycles of the receiver oscillatory reference source;

determining a receiver delta phase in accordance with counts from the receiver first counter and the receiver second counter;

determining ~~from the partially correlated signal~~ the transmitter delta phase ~~and the transmitter second counter count~~ by partially correlating the received signal against at least one of the receive PN component codes;

determining a latency associated with the receiver second counter; and

substantially aligning the ~~receiver~~ receive PN composite code with the ~~transmitter~~ transmit PN composite code in accordance with a first function, the first function

comprising the parameters: the transmitter delta phase, the cycle count of the transmitter second counter ~~count~~, the receiver delta phase, the cycle count of the receiver second counter ~~count~~, and the latency.

25.(Currently Amended) A method as in claim 24 wherein the step of logically combining the at least three receive PN component codes to produce the receive PN composite code ~~further~~ comprises ~~the step of MAND~~ logically combining ~~the at least three~~ four receive PN component codes X, Y, Z_1 and Z_2 according to:

$$(X \oplus (Y \bullet (Z_1 \oplus Z_2))).$$

26.(Currently Amended) A method as in claim 24 wherein the step of logically combining the at least three receive PN component codes to produce the PN composite code ~~further~~ comprises ~~the step of MAJ~~ logically combining ~~the at least three~~ four receive PN component codes X, Y, Z_1 and Z_2 according to:

$$(X \bullet Y) \oplus (X \bullet Z_1) \oplus (X \bullet Z_2) \oplus (Y \bullet Z_1) \oplus (Y \bullet Z_2) \oplus (Z_1 \bullet Z_2).$$

27.(Currently Amended) A method as in claim 24 wherein the step of providing the receiver oscillatory reference source ~~further~~ comprises ~~the step of~~ providing a crystal ~~oscillator~~oscillatory source.

28.(Currently Amended) A method as in claim 24 wherein the step of providing the receiver oscillatory reference source ~~further~~ comprises ~~the step of~~ providing a second atomic reference source.

29.(Currently Amended) A method as in claim 24 wherein the step of substantially aligning the ~~receiver~~receive PN composite code with the ~~transmitter~~transmit PN composite code in accordance with the first function ~~further~~ comprises ~~the steps of~~:

determining an uncertainty chip range associated with the latency associated with the receiver second counter;

moving the ~~receiver generated PN code phases~~phase of the at least three receive PN component codes, other than the at least one ~~receiver~~ receive PN code used for partial correlation, to a predetermined phase within the determined uncertainty chip range; and

searching for full correlation over the uncertainty chip range in units of a number of chips associated with the one ~~receiver~~ receive PN component code used for partial correlation.

30.(Original) A system for generating (PN) spread signals, the system comprising:

a first clock generator;

at least three first pseudo-noise (PN) component code generators coupled to the first clock generator, wherein the first clock generator generates clock signals to drive the PN component code generators;

a logic combiner coupled to the outputs of the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock generator, wherein the first N-bit counter counts the clock signals generated by the first clock generator;

a second clock generator, wherein the second clock generator is adapted to synchronize with the first clock generator; and

a second M-bit counter coupled to the second clock generator, wherein the second M-bit counter counts time since initialization of the second clock generator.

31.(Original) A system as in claim 30 wherein the first clock generator comprises a first direct digital synthesizer.

32.(Currently Amended) A system as in claim 30 wherein the logic combiner comprises a MAND logic combiner that logically XOR combines an output of one of the PN code generators with a logical AND result of at least two other of the PN code generators.

33.(Currently Amended) A system as in claim 30 wherein the logic combiner comprises a MAJ logic combiner that logically XOR combines all logical AND combinations of unique pairs of PN code generator outputs.

34.(Original) A system as in claim 30 wherein the at least three first PN component code generators comprise four first PN component code generators.

35.(Currently Amended) An integrated circuit (IC) comprising~~, wherein the integrated circuit comprises~~:

a first clock signal generator for generating first clock signals;

at least three first pseudo-noise (PN) component code generators coupled to the first clock signal generator;

a logic combiner coupled to the outputs of the at least three first PN component code generators, the logic combiner adapted to generate a composite PN code;

a first N-bit counter coupled to the first clock signal generator, wherein the first N-bit counter is adapted to count the first clock signals;

a second clock generator for generating second clock signals, wherein generating the second clock signals ~~are~~ is synchronized with generating the first clock signals; and

a second M-bit counter coupled to the second clock generator, wherein the second M-bit counter is adapted to count time since initialization of synchronization of generating the second clock signals and generating the first clock signals.

36.(Currently Amended) An IC as in claim 35 wherein the first clock signal generator ~~further~~ comprises a first clock signal input pin.

37.(Currently Amended) An IC as in claim 36 wherein the first clock signal generator ~~further~~ comprises the first clock signal input pin coupled to a first direct digital synthesizer.

38.(Currently Amended) An IC as in claim 35 wherein the second clock generator ~~further~~ comprises a second clock signal input pin.

39.(Currently Amended) An IC as in claim 38 wherein the second clock generator ~~further~~ comprises the second clock signal input pin coupled to a second direct digital synthesizer.

40.(Currently Amended) An IC as in claim 38 wherein the second clock generator ~~further~~ comprises the second clock signal input pin coupled to an atomic clock.

41.(Currently Amended) An IC as in claim 38 wherein the second clock generator ~~further~~ comprises the second clock signal input pin coupled to a crystal oscillator.

42.(Original) An IC as in claim 35 wherein the first clock generator comprises an onboard first direct digital synthesizer.

43.(Original) An IC as in claim 35 wherein the second clock generator comprises an onboard second direct digital synthesizer.

44.(Original) An IC as in claim 35 wherein the second clock generator comprises an onboard first crystal oscillator.

45.(Original) An IC as in claim 35 wherein the IC comprises an Application Specific IC (ASIC).

46.(Original) An IC as in claim 35 wherein the IC comprises a field programmable gate array (FPGA).

47.(Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating and acquiring pseudo-noise (PN) composite spread signals, the method comprising the steps of:

at a transmitter:

providing a PN clock source, the PN clock source having a predetermined cycle rate;

using the PN clock source to generate at least three PN component codes, wherein the step of generating the at least three PN component codes further comprises the steps of:

initializing a first counter, wherein the first counter is adapted to count the PN clock source cycles;

logically combining the at least three PN component codes to produce a PN composite code;

providing an oscillatory reference source, the oscillatory reference source having predetermined cycles;

initializing a second counter, wherein the second counter is adapted to count the cycles of the oscillatory reference source;

determining a transmitter delta phase in accordance with counts from the first counter and the second counter;

PN composite coding the transmitter delta phase and the second counter count;

transmitting the PN composite coded transmitter delta phase and the PN composite second counter count at a predetermined rate;

at a receiver:

receiving the transmitted signal;

partially correlating the ~~transmitted~~ received signal; and

determining a PN composite code slip for chip aligning a receiver PN composite code with the transmitter PN composite code.

48.(Currently Amended) A program storage device as in claim ~~38~~ 47 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.